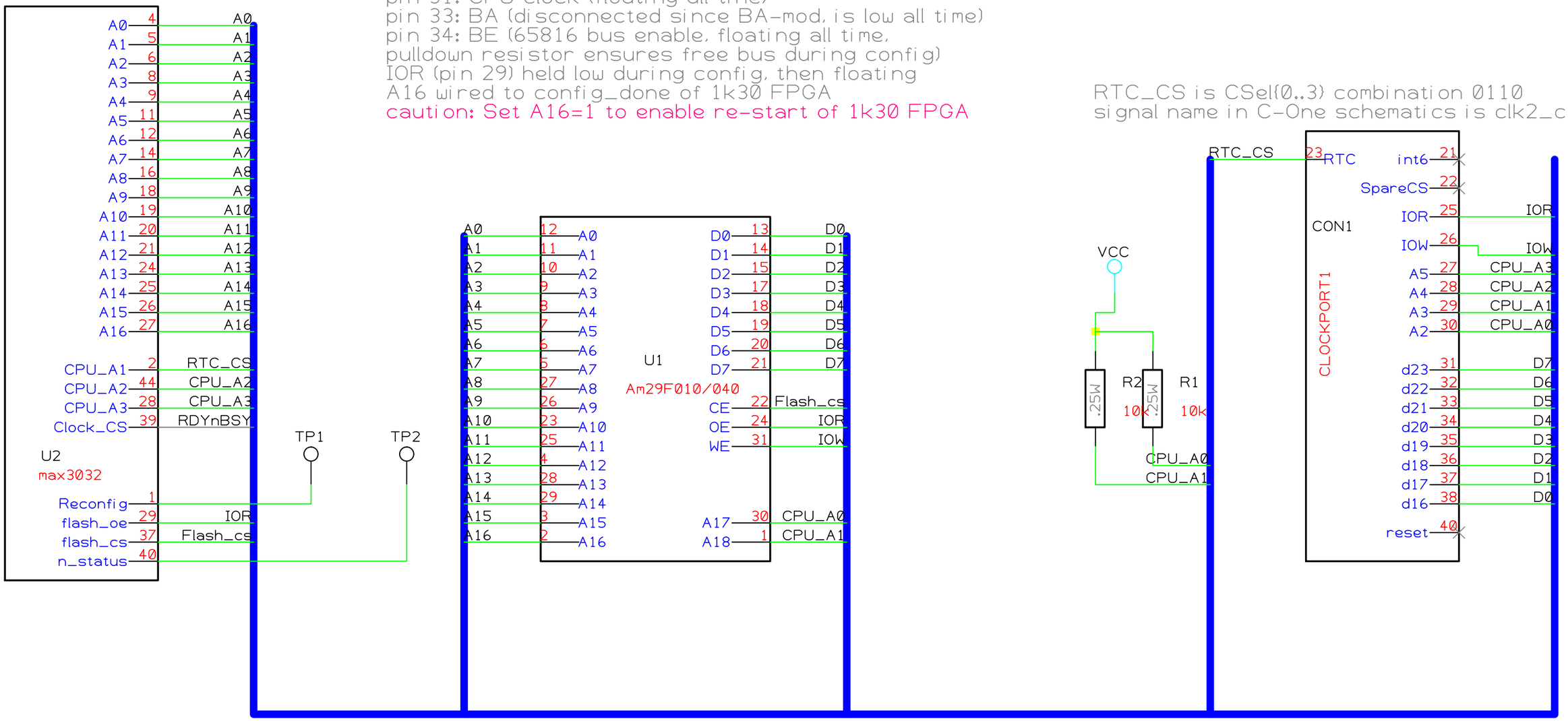
Corrected schematics: June 1st, 2009

for details, refer to the "C-One core development" manual by Peter Wendrich

caution: Chip symbol has wrong signal names, refer to connected signal names only!

more CPLD signals:
pin 41: write pulse for FPGA config
pin 43: 2MHz clock
pin 31: CPU clock (floating all time)
pin 33: BA (disconnected since BA-mod, is low all time)
pin 34: BE (65816 bus enable, floating all time, pulldown resistor ensures free bus during config)
IOR (pin 29) held low during config, then floating
A16 wired to config_done of 1k30 FPGA
caution: Set A16=1 to enable re-start of 1k30 FPGA

RTC_CS is CSel{0..3} combination 0110
signal name in C-One schematics is clk2_cs



TP1 soldered to diodes right next to instant-on board
TP2 soldered to nStatus signal on board (blue wire)
RDYnBSY signal becomes DMA signal of expansion after config
CPLD ignores RDYnBSY while doing config (writes are timed only)
config data is taken from address 0x60000 of flash chip

CPLD waits for nConfig signal, then starts counting through full 64k of flash on power-up, pulsing Flash_CS and pin 41 for every byte, then enters user mode, leaving address counter at A[16..0]=[10000000000]
user mode gives flash access through bottleneck.
set address with reset/count/shift-left, then access flash address